

An Introduction to Boundary Scan (IEEE 1149.1/JTAG)

Detecting PCB defects without physical access

Ensuring the quality of complex printed circuit boards

Over the last decade, testing printed circuit boards (PCBs) to detect defects and ensure product quality has become increasingly difficult. New packaging types like ball grid arrays (BGAs) and other chip-scale packages, as well as dense, exceedingly complex multi-layer board architectures continue to demonstrate the limitations of traditional test techniques during development and manufacturing. When used during manufacturing, in-circuit test (ICT) and other methods that rely on physical access and test points on the PCB can not provide adequate test coverage for today's PCBs. To complement ICT with access-free test, a new test methodology called boundary scan (IEEE 1149.1/JTAG) has emerged.

Why boundary scan?

Why should you consider including boundary scan in your next design? Quite simply, you'll ensure product quality by achieving better test coverage. And that means saving money and time during every phase of a product's life cycle.

- During development, you can cut weeks off of prototype debug. And, instead of programming devices off-board, which can be time-consuming and inflexible, programmable logic and flash memories can be programmed after they've been affixed to the PCB and easily re-programmed as design changes dictate.
- During manufacturing, defects, which are impossible for ICT systems to detect, are quickly identified and diagnosed. And ICT fixturing costs will be reduced significantly as more tests are performed with boundary scan.
- After market rollout, fast troubleshooting in the field can find board faults rapidly and ensure customer satisfaction.

What is boundary scan?

The boundary-scan standard has been designed into most digital integrated circuits (ICs). When these ICs are attached to a boundary-scan path, an embedded communication bus on the PCB is created and wide range of benefits becomes available. Boundary scan can be used to test the quality of the PCB assembly, to program devices for design verification after they have been soldered to the board and to access the internal structures of ICs to help verify the design. Many types of IC packages, such as ball grid arrays (BGAs) deny physical access to test probes because the point of contact between the device and the PCB is beneath the device. Boundary scan is the only method that can ensure the quality of the manufacturing process by testing to determine whether devices are properly attached to the PCB and whether the interconnections between devices on the PCB will carry a quality electrical signal.

What is ASSET InterTech's ScanWorks™ environment?

The intuitive and easy-to-use ScanWorks boundary-scan test and in-system programming environment from ASSET InterTech has established itself as the market leader in sophisticated test and programming tools. The PC-based ScanWorks environment can be configured as a Test Development Station, Manufacturing Station, Diagnostic & Repair Station or Programming Station. A worldwide network of technical test engineers supports ScanWorks. ASSET's services division, Ensure DFT (EDFT™), provides high-level design-for-test and programming services. For more information, visit our web site a www.asset-intertech.com, call 888-694-6250, send faxes to 972-437-2826 or direct email to sales@asset-intertech.com.