

DEBUG PORT DESIGN GUIDELINES

This document provides information on designing debug ports for different processor types, either by providing links to the processor vendor's recommendations, or by detailed descriptions if recommendations are not available from the vendors.

Note: The lists of mandatory signal/pin connections are those required by our Processor-Controlled Test (PCT) Test and Debug Solutions – other uses of the debug ports may need additional connections.

INTRODUCTION

Traditionally, low-level microprocessor code was debugged using an emulator. An emulator is an instrument that replaces a socketed processor, and provides the developer with the debug functions to download code, set breakpoints, single step code, and so on.

As processor speed increased, it became impossible to design emulators of this type, so CPU vendors began to embed the debug functions on the processor die. Typically, these functions are accessible via the JTAG port, but in some cases proprietary interface pins are used (e.g. Freescale™ BDM).

CPU vendors use different naming conventions for their debug interfaces, but throughout this document, the term debug port is frequently used as a generic term.

A debug port is typically an on-board connector or series of test points that link to a set of test/debug pins on the processor package. If JTAG is used, it consists of the 5 JTAG signals and 0-3 other signals. The number of additional sideband signals required depends on the processor type.

INTEL® PROCESSORS (PROCESSOR-CONTROLLED TEST 304X)

Processors relevant to this section:

- Intel® Pentium® 4 processor FC-PGA (423 pin)
- Intel® Pentium® 4 processor µFC-PGA (478 pin)
- Mobile Intel® Pentium® 4 Processor-M (478 pin)
- Intel® Pentium® M processor - Centrino™ (478 pin)
- Intel® Celeron® processors based on the above cores
- Intel® Xeon® processor INT-µPGA (603 pin)
- Intel® Xeon® processor FC-µPGA2 (604 pin)
- Intel® Xeon® processor FC-µPGA2 (604 pin)
- Intel® Atom™ Nxxx/Exxx FC-BGA (676 pin)
- Intel® Atom™ Zxxx T-PBGA (518 pin)
- Intel® 2nd Generation Core® processor i3/i5/i7 LGA1156 (1156 pin)
- Intel® 2nd Generation Core® processor i7/55xx/56xx LGA1366 (1366 pin)
- Intel® 2nd Generation Xeon® processor E3/E5 Socket R (2011 pin)

Design guidelines for debug ports:

- Processor-Controlled Test 304x Design-for-Test – See DFT304x document at the following address:

<http://www.asset-intertech.com/Products/Processor-Controlled-Test/PCT-Software.aspx#PCTResources>

If your board has a 60-pin male debug header (XDP), then you can use this by inserting the POD-II adapter supplied by us.



Illustration 5. 60-pin male debug port header (XDP)

If your board does not have a header, but has a socketed processor, you can use one of our interposer products. An interposer is a break-out PCB that sits between the processor and the socket. The POD-II is required to condition signals – this is plugged into the interposer, as shown in Illustration 6.



Illustration 6. Processor Socket and Interposer

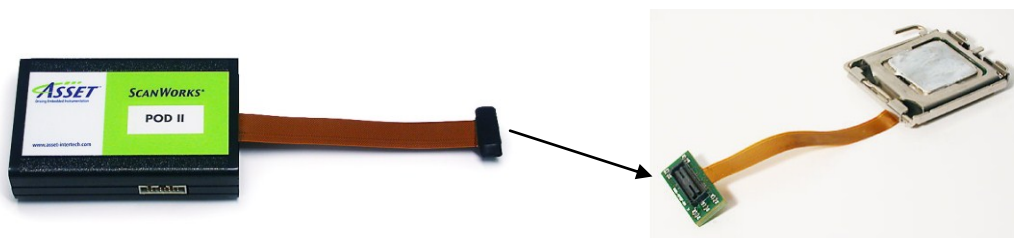


Illustration 7. POD-II and Interposer

If your processor is soldered, and your board does not have a debug header, then you will have to construct a simple test jig to get access to the appropriate test points (Illustration 2). Contact us if you require assistance with this. Although, the debug port specification defines a 26-pin connector (or 60 pin in the case of XDP), the pins required for the operation of PCT Test and Debug solutions are:

XDP Pin	Signal Name	XDP Pin	Signal Name
1 ₃	GND	2	GND
3	OBS_FN_A0 (PREQ#)	4 ₁	OBS_FN_C0
5	OBS_FN_A1 (PRDY#)	6 ₁	OBS_FN_C1
7	GND	8	GND
9	OBS_DATA_A[0]	10	OBS_DATA_C[0]
11	OBS_DATA_A[1]	12	OBS_DATA_C[1]
13	GND	14	GND
15	OBS_DATA_A[2]	16	OBS_DATA_C[2]
17	OBS_DATA_A[3]	18	OBS_DATA_C[3]
19	GND	20	GND
21 ₁	OBS_FN_B0	22 ₁	OBS_FN_D0
23 ₁	OBS_FN_B1	24 ₁	OBS_FN_D1
25	GND	26	GND
27	OBS_DATA_B[0]	28	OBS_DATA_D[0]
29	OBS_DATA_B[1]	30	OBS_DATA_D[1]
31	GND	32	GND
33	OBS_DATA_B[2]	34	OBS_DATA_D[2]
35	OBS_DATA_B[3]	36	OBS_DATA_D[3]
37 ₃	GND	38	GND
39 ₂	HOOK0 (PWRGOOD)	40	HOOK4 (BCLK0)
41	HOOK1	42	HOOK5 (BCLK1)
43	VCC_OBS_AB	44	VCC_OBS_CD
45	HOOK2	46	HOOK6 (RESET#)
47	HOOK3	48	HOOK7 (DBR)
49 ₃	GND	50	GND
51	SDA	52	TDO
53	SCL	54	TRSTn
55	TCK1	56	TDI
57	TCK0	58	TMS
59 ₃	GND	60	XDP Present

FreeScale™ PowerArchitecture™/IBM® PowerPC™ - COP (Processor-Controlled Test 4031)
Processors relevant to this section:

- Freescale™ PowerArchitecture™ 740/745/750/755
- Freescale™ PowerArchitecture™ 603e (200-300 MHz)
- Freescale™ PowerArchitecture™ 7400/7410/7450/7447A/7448/7455/7457, etc.
- Freescale™ PowerQUICC™ II 82xx
- Freescale™ PowerQUICC™ II Pro 83xx
- Freescale™ PowerQUICC™ III 85xx
- Freescale™ PowerQUICC™ III 8640/40D/41/41D
- IBM® PowerPC™ 750 DD2/DD3
- IBM® PowerPC™ 750 CX DD1/DD2
- IBM® PowerPC™ 750 FX DD1/DD2
- This list may be incomplete – see our website for the latest status:

The PowerPC™ Common On-Chip Processor (COP) debug port uses the processor's JTAG bus and some additional signals.

Design guidelines for COP debug ports:

- Processor-Controlled Test 4000 Design-for-Test. See DFT4000 document at the following address:
<http://www.asset-intertech.com/Products/Processor-Controlled-Test/PCT-Software.aspx>
- See the reference manual for your specific processor, e.g. “MPC5200 Hardware Specifications”. Search for “MPC5200” on the Freescale™ website if the link below doesn’t return the document:
http://www.freescale.com/files/32bit/doc/data_sheet/MPC5200.pdf?srch=1

If your board has a debug header, which is designed following the above specification, then you can plug directly into this.

If your processor is soldered, and your board does not have a debug header, then you will have to construct a simple test jig to get access to the appropriate test points (Illustration 2). Contact us if you require assistance with this.

Although the PowerPC™ COP debug port specification defines a 16-pin connector, the pins required for the operation of PCT Test and Debug solutions are:

Debug Port Pin No.	Signal
1	TDO
3	TDI
4	TRST
6	VDD
	TCK
9	TMS
12	GND
13	HRST

FREESCALE™ POWERARCHITECTURE™ PROCESSORS – BDM (PROCESSOR-CONTROLLED TEST 4033, 4034)

Processors relevant to this section:

- Freescale™ PowerArchitecture™ 5xx Family
- Freescale™ PowerArchitecture™ 8xx Family

The PowerArchitecture™ Background Debug Mode (BDM) debug port uses a proprietary 3-pin bus with additional signals.

Design guidelines for PowerArchitecture™ BDM debug ports:

- Processor-Controlled Test 4000 Design-for-Test. See DFT4000 document at the following address:
<http://www.asset-intertech.com/Products/Processor-Controlled-Test/PCT-Software.aspx>
- See the reference manual for your specific processor, e.g. Application Note AN2387/D, titled “MPC8xx Using BDM and JTAG”. Search for “AN2387” on the Freescale™ website if the link below doesn’t return the document:
http://www.freescale.com/files/netcomm/doc/app_note/AN2387.pdf

If your board has a 10-pin BDM debug header, which is designed following the above specification, then you can plug directly into this.

If your processor is soldered, and your board does not have a debug header, then you will have to construct a simple test jig to get access to the appropriate test points (Illustration 2). Contact us if you require assistance with this.

Although the PowerArchitecture™ BDM debug port specification defines a 10-pin connector, the pins required for the operation of PCT Test and Debug solutions are:

Debug Port Pin No.	Signal
1	VFLS0
3	GND
4	DSCLK
6	VFLS1
7	HRESET
8	DSDI
9	VDD
10	DSDO

ARM® 7/9 PROCESSORS AND CORES (PROCESSOR-CONTROLLED TEST 4071)

Processors relevant to this section:

- ARM® 7 processors
- ARM® 9 processors
- Any processor based on ARM®7/9 cores, such as the following:
- Cirrus Logic® EP9xxx Embedded Processors
- Conexant® ARM®7/9 networking SoC's
- Freescale™ MAC7100 family (Automotive)
- OKI Semiconductor ARM®-based MCU's

The ARM® debug port uses the processor's JTAG bus, and some additional signals.

Design guidelines for ARM® debug ports:

- Processor-Controlled Test 4000 Design-for-Test. See DFT4000 document at the following address:
<http://www.asset-intertech.com/Products/Processor-Controlled-Test/PCT-Software.aspx>
- ARM® Multi-ICE guidelines. The following User Manual contains a section that describes the debug port:
http://hwbb.googlecode.com/svn/trunk/CPU/ARM/DATASHEET/ARM9/DUI0048F_MICE2_2.pdf

If your board has a 20-pin debug header that is designed following the above specification, then you can plug directly into this.

If your processor is soldered, and your board does not have a debug header, then you will have to construct a simple test jig to get access to the appropriate test points (Illustration 2). Contact us if you require assistance with this.

Although, the ARM® debug port specification defines a 20-pin connector, the pins required for the operation of PCT Test and Debug solutions are:

Debug Port Pin No.	Signal
1	VTref
3	nTRST
4	GND
5	TDI
7	TMS
9	TCK
13	TDO
15	nSRST

IBM® POWERPC™ 4XX CORES

Processors relevant to this section:

- IBM® PowerPC™ 405xx family of embedded cores
- IBM® PowerPC™ 440xx family of embedded cores

The IBM® 4xx 16-pin debug port uses the processor's JTAG bus, and some additional signals.

Design guidelines for these debug ports:

- Processor-Controlled Test 4000 Design-for-Test. See DFT4000 document at the following address: <http://www.asset-intertech.com/Products/Processor-Controlled-Test/PCT-Software.aspx>
- Obtain manual from IBM®, e.g. "PowerPC 405 Processor Core User Guide" (publication no. SA14-2764-00). Search for "ppc405fx_um" on the IBM® website if the link below doesn't return the document:

<http://www-01.ibm.com/chips/techlib/techlib.nsf/techdocs/D060DB54BD4DC4F2872569D2004A30D6>

If your board has a 16-pin debug header, which is designed following the above specification, then you can plug directly into this.

If your processor is soldered, and your board does not have a debug header, then you will have to construct a simple test jig to get access to the appropriate test points (Illustration 2). Contact us if you require assistance with this.

Although, the IBM® debug port specification defines a 16-pin connector, the pins required for the operation of PCT Test and Debug solutions are:

Debug Port Pin No.	Signal
1	TDO
3	TDI
4	TRST
6	Power Sense
7	TCK
9	TMS
16	GND

ASSET CONTACTS:

Please contact your ScanWorks sales representative for more information.

ASSET InterTech, Inc.
2201 N. Central Expy., Ste 105
Richardson, TX 75080
+1 888 694-6250 or +1 972 437-2800
<http://www.asset-intertech.com>