ScanWorks®
Platform for Embedded Instruments

4-Day ScanWorks® Boundary-Scan Test Workshop Details

Class Administration Plan

- Class starts at 8:00 a.m. and ends at 5:00 p.m. each day
- Lunch is 60 minutes
- 2 breaks in the morning and 2 breaks in the afternoon

Day 1

Section 1: Introduction

Class Information
ScanWorks® hardware, software, and support
Boundary-scan 101 tutorial (The Concept, 1149.1 Details, DFT Guidelines for Boundary-Scan)

Section 2: Class Hardware

The ScanLite2™ Board

Section 3: Overview of the ASSET Test Development Process

Section 4: Getting Started With ScanWorks®

Touring the ScanWorks Dialog Box
Assembly Test ScanWorks Actions
Program ScanWorks Actions
Utility ScanWorks Actions
Legacy ScanWorks Actions
Touring the Menu Options

Section 5: Describing a Design

What Do I Need to Describe My Design?
Using the Design Wizard and the Scan Path Discovery capabilities
Terminology

Section 6: Netlists in the ScanWorks® Flow

When is a Netlist Required?
Netlist Formats Accepted by ScanWorks
Specific PCB Layout Files and Schematic Files Accepted by ScanWorks
Importing and Translating a Netlist
Specifying Power and Ground Nets
Modeling Non-Boundary-Scan Devices
Inputs and Outputs to the Netlist Step

Day 2

Section 7: Scan Path Verification

Procedure for Creating a Scan Path Verify Action

Building, applying, and diagnosing with the Scan Path Verify Action
Tips and Tricks
Inputs and Outputs to Scan Path Verify Actions

Section 8: Interconnect Testing

Interconnect Action Facts
Quick Steps to Create an Interconnect Action
The Fault Coverage Report and other Reports Generated
Running an Interconnect Action Against Hardware
Diagnostic Reports and Isolating Faults
Viewing Faults in a Schematic or Layout
Inputs and Outputs to the Interconnect Action

Section 9: Memory Access Verification

Current Practice in Memory Testing
Automated Static Memory Tests
Creating a Memory Access Verify Action
Memory Device Cross References
Learning About Memory Models
Building Your Memory Access Verify Action
Configuring Access to Memory Devices
Apply MAV Vectors to Hardware
Diagnosing Faults with the Memory Access Verify Action
Interactive Memory Debug and Diagnostic Capabilities
Inputs and Outputs to Memory Access Verify Actions

Day 3

Section 10: The Flash Action

Creating Flash Actions
What a Flash Action Does
Quick Steps to Create Flash Actions
Selecting Flash Targets
Creating Cross References to Flash Devices
Defining a Flash Action
Image Data Files
Configuring Access to a Flash Device
Flash Options and Issues
Building and applying a Flash Action
Reports that are generated
Tips and Tricks
Inputs and Outputs to Flash Actions

Section 11: Macros

Characteristics of the Macro Language
Applications of Macros
The Macro Language Library

Using buses to simplify macro development
A Macro Example

Section 12: Deploying to Manufacturing

Sequences
Exporting and Importing Projects
Setting Levels of Access

Day 4

Section 13: Tutorial On Using The Design Browser

Section 14: Scan Path Verify Debug and Diagnostics

Interpreting SPV Diagnostic Messages
Using The SPV Debug Capabilities

Section 15: Interconnect Debug and Diagnostics

Interpreting Interconnect Diagnostic Messages
Using the Interconnect Debug Capability

Section 16: Memory Access Verify Debug and Diagnostics

Interpreting MAV Diagnostics Messages
Using The Interactive Memory (Debug) Capability

Section 17: Flash Debug and Diagnostics

Interpreting Flash Diagnostic Messages
Using the Interactive Flash (Debug) Capability