SourcePoint® 7.12 Release Notes

Content

Contact Us

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Requirements

Host Operating Systems Supported
Windows 10, 11
Recommended Configuration: Multicore Intel or AMD processor, 2GHz or faster; 16GB RAM; 256GB SSD

Note: You may need to contact your systems administrator to gain **administrator privileges** on your host computer to properly install SourcePoint. The Installation wizard may give errors when administrator privileges are not enabled.

New Features and Errata

Version 7.12 Build 68 – March, 2025

This is our biggest release yet! It has the following major enhancements:

- Arrow Lake support
- Meteor Lake AAEON UP Xtreme i14 board DCI support
- Jasper Lake KINGDEL M6 board DCI support
- New VMCS fields for SEAM VMX non-root operation

- Multiple debugger support (WinDbg + SourcePoint) – HV, SK, NTOS

As well, there are well over 40 fixes and minor enhancements in this release:

Number	Summary	Failure mode	Priority
16947	Document VMX indicator in status bar	Missing functionality	Normal
16946	Update Register view documentation	Missing functionality	Normal
16945	WHL NPW Identify target not working	Malfunction	Normal
16944	Add separate TC file for Kingdel JSL board	Suggested improvement	Normal
16939	Add VMCS register schema to JSL	Suggested improvement	Normal
16938	change register window to sort by name as default.	Suggested improvement	Low
16936	LoadCurrent not finding symbols for ntkrnlmp in 7.12.67	Malfunction	Normal
16935	debug build of 64bit AssetDCI crash with use of bad pointer. no problem with release build.	Emulator crash	Normal
16933	JSL: Step fails after SMM entry breakpoint	Malfunction	Normal
16931	AAEON_ADL: Gettng warning when TraceHub.mac is loaded in command window	Missing functionality	Normal
16930	JSL(EHL): Issue with step on DCI	Run Control Failed	High
16927	CFL-H,CFL-U DCI: Target identify not working with 7.12.66	Malfunction	High
16926	add bitmaps on legacy MSR (MSR_)LBR_INFO_x	Suggested improvement	Normal
16925	New bitmaps in CR3 and CR4	Suggested improvement	Normal
16924	Differentiate SEAM VMX from VMX modes	Missing functionality	Customer Requirement
16923	Add new VMCS fields for SEAM VMX non-root operation	Missing functionality	Customer Requirement
16922	Show BaseName+ Offset in disassembly when WinDbg LoadCurrent macro has detected base address but not loaded Symbols	Suggested improvement	Customer Requirement
16919	WinDbg: Flashing windows when starting SP and running LoadCurrent macro	Cosmetic	Normal
16918	WinDbg: SP can't find cached symbols	Malfunction	Normal
16917	WinDbg: VM Launch does not work on E-cores	Malfunction	Normal
16916	WinDbg: E-core stopped in NT kernel shows Host mode instead of Guest mode	Malfunction	Normal

16914	WinDbg: IPT conceal bits need to be cleared by FW rather than by SP	Missing functionality	Normal
16912	Enhancement for LoadCurrent macro	Suggested improvement	Normal
16911	Identify Target selects wrong TC file with AAEON Alder Lake target	Malfunction	High
16910	Symbol view Find dialog opens small the first time	Malfunction	Normal
16909	Find in Symbol view doesn't open dialog from item of not symbol like "Labels", "Data"	Suggested improvement	Low
16908	Tooltip in open space in the Code view	Malfunction	Low
16907	Viewpoint view does not remember column widths	Malfunction	Normal
16906	display FSBASE and GSBASE in General MSR page	Suggested improvement	Normal
16905	Add a text column to IDT tab in descriptors view	Suggested improvement	Normal
16903	Starting SP with the PCI devices view open halts the target	Incorrect Functionality	Normal
16902	Redirect LoadCurrent output to the Command view	Suggested improvement	Normal
16900	JSL Targets do not have good run control via DCI connection	Run Control Failed	Customer Requirement
16896	Changing viewpoint causes register view to switch from VMCS to General regs with hetero target	Suggested improvement	Normal
16895	Add horizontal scrollbar to register view	Suggested improvement	Normal
16888	AAEON-TGL: Getting no DBc trace after collecting MTb.	Missing functionality	High
16887	AAEON-ADL(celeron): System and DBc traces not working. MTB looks Ok.	Missing functionality	High
16886	AAEON-ADL(celeron): Threads P4-P7 running after SP reset	Missing functionality	Normal
16882	ARL-S DCI: Run control unstable with SP 7.12.63	Run Control Failed	High
16879	Change order of Symbol search options	Suggested improvement	Low
16872	Register window fails to restore which group was expanded from project file	Malfunction	Low
16846	HV Debugger and SP running at the same time crashes the target (WinDbg)	Incorrect Functionality	High
16841	MTL-P_2 DCI: Target identify not working. XDP3e works	Malfunction	High
16828	Pressing Refresh in Intel PT Trace view hangs SP	SP hang	Normal
16810	SourcepointEXDI.dll to cache bad memory requests	Suggested improvement	Normal

16473	Validate TH trace on RPL	Suggested improvement	Normal
16395	Validate LBR / Intel PT on SRF	Suggested improvement	Normal
16389	Validate TH trace on MTL	Suggested improvement	Normal

There are still open errata that will be addressed in an upcoming release:

Number	Summary	Failure mode	Priority
16950	Intel PT not working across VMX transitions on E-cores	Malfunction	High
16943	AAEON-ADL(celeron): DBc traces not working. MTB looks Ok.	Missing functionality	High
16941	Need to sign other exe's in SP distribution	Missing functionality	Normal
16934	DbC Connection App displays file version rather than driver version	Suggested improvement	High
16932	Add support for Linear Address Masking (LAM)	Missing functionality	Normal
16929	Add overwrite mode to LBR trace	Suggested improvement	Normal
16876	ADL C-State handling not working correctly	Malfunction	High
16873	timeBeginPeriod() is not effective with windows 11	Suggested improvement	Normal
16864	MTL-P_2 XDP3e/Dci: Target reset not working	Missing functionality	High
16863	ARL XDP3e/Dbc: Target didn't stop at reset vector after SP Reset target	Missing functionality	High
16862	ARL DbC: Getting no data available while collecting LBR, BTS and IPT traces and breaks run control	Malfunction	Normal
16829	Intel PT Trace: Log shows memory map errors when they are really page translation errors	Incorrect Functionality	Low
16820	WinDbg: Trace Save As is slow	Suggested improvement	Low
16791	LoadCurrent fails in User Space	Malfunction	Normal
16787	ICX: AET trace not working with 7.12.51. STM works fine.	Malfunction	High
16780	Single step fails on VMRESUME instruction with TFlag Turned off error	Suggested improvement	Normal
16775	WinDbg Break in the Secure Kernel causes loss of control	Run Control Failed	Normal
16762	Add support for Panther Lake (PTL)	Suggested improvement	Normal
16761	Validate LBR / Intel PT trace on PTL	Suggested improvement	Normal
16701	CFL-H/DCI: SP loses run control while stepping ocassionally	Malfunction	Normal

16698	GNR: SP connects fine but stuck in "Acquiring CPU Assets" when target is power cycled.	Malfunction	High
16689	WinDbg: Software BPs hang WIndows on CML-U (when lazy acquire is enabled)	Malfunction	High
16687	MTL: TCO timer disable macro not working	Missing functionality	High
16676	On GNR(SRF) SP takes very long time to connect to target on first project load after SP is loaded	Incorrect Functionality	High
16671	Lazy Acquire Not Working with all processor hardware breakpoint in older projects	Suggested improvement	Normal

To see the current status and differences between current offerings of open chassis (ECM-XDP3e) debug and closed chassis (DCI/DbC) debug, please refer to the following tables:

ECM-XDP3e:

	Run-Control	LBR	BTS (to system memory	Intel PT (to system memory)	UEFI and ME message trace (thru Trace Hub) to memory and MTB	AET (thru Trace Hub) to memory, MTB
SERVER & WORKSTATION						
Skylake Server	√	√	√	√	√	√
Cascade Lake Server	√	√	√	√	√	√
Ice Lake Server	√	√	√	√	√	√
Sapphire Rapids	√	√	√	√	√	√
Fish Hawk Falls	√	√	√	√	√	√
ICX-D	√	√	√	√	X	X
Emerald Rapids	√	√	√	√	O	O
Granite Rapids	√	√	√	√	O	O
Sierra Forest	√	√	√	√	O	O
CLIENT						
Skylake Client	√	√	√	√	√	√
Kaby Lake Client	√	√	√	√	√	√
Amber Lake Client	√	√	√	√	√	√
Coffee Lake Client	√	√	√	√	√	√
Whiskey Lake Client	√	√	√	√	√	√
Cannon Lake Client	√	√	√	√	√	√
Ice Lake Client	√	√	√	√	√	√
Comet Lake Client	√	√	√	√	√	√

Tiger Lake Client	√	√	√	√	√	√
Jasper Lake	√	√	√	√	X	X
Elkhart Lake	√	√	√	√	X	X
Rocket Lake	√	√	√	√	√	√
Alder Lake	√	√	√	√	√	√
Raptor Lake	√	√	√	√	√	√
Meteor Lake	√	√	√	√	√	√
Arrow Lake	√	√	√	√	O	O

√ In current release
O In Upcoming release
X Not supported

DCI/DbC:

	Run-Control	LBR	BTS (to system memory	Intel PT (to system memory)	UEFI and ME message trace (thru Trace Hub) to memory and MTB	AET (thru Trace Hub) to memory, MTB	UEFI and ME message Trace (thru Trace Hub) to DCI/ DbC Streaming Trace	AET (thru Trace Hub) to DCI/ DbC Streaming Trace
SERVER & WORKSTATION								
Skylake Server	X	X	X	X	X	X	X	X
Cascade Lake Server	X	X	X	X	X	X	X	X
Ice Lake Server	√	√	√	√	√	√	X	X
Sapphire Rapids	X	X	X	X	X	X	X	X
Fish Hawk Falls	X	X	X	X	X	X	X	X
ICX-D	√	√	√	√	X	X	X	X
CLIENT								
Skylake Client	X	X	X	X	X	X	X	X
Kaby Lake Client	X	X	X	X	X	X	X	X
Amber Lake Client	X	X	X	X	X	X	X	X
Coffee Lake Client	√	√	√	√	√	√	√	√
Whiskey Lake Client	√	√	√	√	√	√	√	√
Cannon Lake Client	√	√	√	√	X	X	X	X
Ice Lake Client	√	√	√	√	√	√	√	√
Comet Lake Client	√	√	√	√	√	√	√	√

Tiger Lake Client	√	√	√	√	√	√	√	√
Jasper Lake	√	√	√	√	X	X	X	X
Elkhart Lake	√	√	√	√	X	X	X	X
Rocket Lake	√	√	√	√	√	√	√	√
Alder Lake	√	√	√	√	√	√	√	√
Raptor Lake	√	√	√	√	√	√	√	√
Meteor Lake	√	√	√	√	√	√	√	√
Arrow Lake	√	√	√	√	√	O	O	O

√ In current release
O In Upcoming release
X Not supported

Notes:

Run-Control: standard Halt, Go, Single-Step, etc. commands.

LBR: Last Branch Record uses MSRs.

BTS: Branch Trace Store uses system memory.

Intel PT: Processor Trace uses system memory.

UEFI, AET and ME message trace use the Trace Hub, and can deliver trace data to system memory, MTB, or (with DCI DbC support) Streaming Trace out of reset.
MTB is Memory Storage Controller Trace Buffer and captures trace data directly from reset. This buffer is typically 2kB - 8kB in size.

Version 7.12 Build 63 – November, 2024

This build has the following major enhancements:

- Alder Lake AAEON UP Xtreme i12 (Alder Lake) support
- SSP (Shadow Stack Pointer) register added
- Descriptor view enhancements
- Meteor Lake/Arrow Lake DCI support
- Arrow Lake Intel Processor Trace
- Allow sorting of MSR and VMCS names and numbers in register displays
- Windows debug stability enhancements
- Display MSR names in AET display

The issues resolved in this release are as follows:

Number	Summary	Failure mode	Priority
16871	Register windows crash with click on value of MSR/VMCS while running	SP crash	High
16870	ADL/MTL/SRF/ARL Bit 63 omitted when reading PDR on little cores	Malfunction	Must Fix

16869	Add support for SSP register	Missing functionality	Normal
16868	WinDbg: Validate support for AAEON ADL i7 board	Suggested improvement	High
16861	WinDbg: Hit VM Launch BP, Intel PT does not show vmlaunch instruction at end of trace	Malfunction	Normal
16856	WinDbg: Intel PT shows extra instructions at end of trace	Malfunction	Normal
16854	WinDbg: stack unwind with kernel symbol part 2	Suggested improvement	Normal
16853	Ignore CR3 with symbol address	Suggested improvement	Normal
16851	WinDbg: VM Resume in early boot	Malfunction	Customer Requirement
16849	WinDbg: Always break on VM launches and rewrite debug registers	Suggested improvement	High
16848	Failed to find section table of pdb file winload_prod.pdb	Missing functionality	Normal
16844	AET Trace: Display MSR name on MSR events	Suggested improvement	Normal
16843	AET Trace: MSR RD/WR values are missing the upper 32 bits	Malfunction	Normal
16842	SP should close WinDbg	Suggested improvement	Normal
16840	ARL: need arl_dbc tc file	Suggested improvement	High
16838	Open a second Trace view: Symbols are off	Malfunction	Normal
16836	WinDbg: Trap flag sometimes not cleared in HV/VBS	Incorrect Functionality	Normal
16833	WinDbg: Codeview does not display disassembly at RIP after a VMLaunch BP into Secure Kernel	Malfunction	Normal
16815	Register view: Allow sorting by register name/number in MSR/VMCS groups	Suggested improvement	Normal
16799	WinDbg: Validate support for AAEON ADL Celeron board	Suggested improvement	High
16788	Vmresume break with Intel PT enabled crashes the target	Malfunction	High
16723	MTL: Target Identify not working	Missing functionality	High
16674	Production ASSETDCI.exe crashes when SP connects. Running in Windows 8 compatibility mode solves this	Emulator crash	High
16633	Validate DbC on ARL	Suggested improvement	High
16630	Validate LBR / Intel PT trace on ARL	Suggested improvement	High
16390	Validate DbC on MTL	Suggested improvement	High

Version 7.12 Build 59 – July, 2024

This build has the following major enhancements:

- Sierra Forest 2P validated
- Arrow Lake support
- VM Resume breakpoint added
- New Intel PT feature: PTWRITE
- VM Exit breakpoint bit labels
- VMCS Viewer/Editor new feature
- Page table entry caching
- Clear Intel PT conceal bits
- WinDbg stack display
- Demangled names

All TTs from 7.12.47 as listed below have been addressed, with exception of WinDbg support for AMD (TT-16739).

The issues resolved in this release are as follows:

Number	Summary	Failure mode	Priority
16832	WinDbg: Intel PT shows too many instructions at end of trace after VM Exit breakpoint	Malfunction	Normal
16831	WinDbg: Intel PT shows too many instructions on first single step after VM entry transition	Malfunction	Normal
16830	AET and Intel PT don't align on first trace capture	Malfunction	Normal
16827	WinDbg: Add progress dialog for time aligning trace	Suggested improvement	Normal
16824	AET scrolling issue	Malfunction	Normal
16817	Remove prefixes from Intel MSR names	Suggested improvement	Normal
16814	Register view: Fix FindMSR with new VMCS register groups	Suggested improvement	Normal
16811	WinDbg Classic bug: Reads memory at old RIP value - Add page table entry caching for performance	Incorrect Functionality	High
16808	Cache value of GSBASE to improve performance	Suggested improvement	Normal
16807	SourcepointEXDI.dll truncated CRn/DRn values to 32bit	Malfunction	Normal
16806	Change Trace view Symbols setting to default to enabled	Suggested improvement	Normal
16805	WinDbg: Intel PT programming code should clear IPT conceal bits in VMCS	Suggested improvement	High
16801	WinDbg: Add support for demangling MS names	Suggest improvement	Normal
16797	Failed to load hardware breakpoint from project file when loading project while target is running	Malfunction	Normal
16796	WinDbg: HW BP set via WinDbg remains set in SP	Malfunction	High
16795	WinDbg: BP icons sometimes missing from Code view	Malfunction	High
16790	LoadCurrent macro scans forever	Malfunction	Normal

16786	Setting VMEXIT break from command line defaults data to 0	Incorrect Functionality	Normal
16783	Add VM command which would show VM status "Off","Guest","Host"	Suggested improvement	Normal
16782	WinDbg: Add VM exit reason to the cause command	Suggested improvement	High
16779	Add VMRESUME(VMENTRY) breakpoint	Suggested improvement	Normal
16776	WinDbg: Intel PT and LBR failures in secure kernel and hypervisor	Malfunction	Normal
16774	WinDbg: AET only partially works with HV/VBS enabled	Malfunction	Normal
16771	Add VM Exit reason labels to VM Exit Breakpoint data mask	Suggested improvement	Normal
16770	SourcePoint not running Event macros if parsed from WinDbg	Malfunction	High
16767	WinDbg .reload command fails with multiple unknown module names	Malfunction	High
16756	WinDbg: Add support for stack unwind with kernel symbols	Suggested improvement	Normal
16747	Bring SP to fore when any message boxes are presented during WinDbg	Suggested improvement	Normal

Version 7.12 Build 47 – December, 2023

Our latest build has the following major enhancements:

- **Integration of WinDbg Windows debugger with SourcePoint using EXDI**
- Full Meteor Lake support
- Sierra Forest support
- Enhancements to use of .ini file for directory updates on Project, Macro, etc. loading
- Fix for Ice Lake server Trace Hub support
- Dwarf5 symbols support
- Guard Bit support for hardware debug registers

The major enhancement in this release is the support for the WinDbg Windows debugger. The new SourcePoint WinDbg product complements WinDbg with SourcePoint's JTAG-based capabilities: many more breakpoint types (SMM entry/exit/data access, machine check, etc.); Intel Processor Trace; Architectural Event Trace (AET); etc.; for powerful insight into the Windows kernel.
For more information on this product, check out the SourcePoint Academy: https://www.asset-intertech.com/resources/academy/sourcepoint-academy/.

There are still open errata that will be addressed in an upcoming release. "TT" is short for "Trouble Ticket":

TT-16740	**WinDbg**: Break after running StartWinDbgExdi.mac sometimes hangs
TT-16739	**WinDbg**: Need to validate on AMD target
TT-16730	**ALL**: Intel PT Call Chart sometimes reports timestamp not recorded
TT-16729	**WinDbg**: SP and WinDbg show different IP values when VBS enabled
TT-16728	**WinDbg**: Add support to load all symbols, as opposed to just at current IP
TT-TBD	**WinDbg**: .reload page translation failures
TT-TBD	**WinDbg**: Add LoadAll.mac for all symbols
TT-16714	**ADL**: Power cycle always stops at reset vector
TT-16664	**EMR**: GUI target reset not working (but power cycle and reset work)
TT-16656	**RPL**: No AET, SW/FW trace when set to system memory. MTB works
TT-16612	**EMR**: Full validation of Trace Hub on EMR, GNR
TT-16601	**ALL**: Watch and Symbols view sometime show extraneous data
TT-16588	**ALL**: Add ZMM register view for Intel
TT-16399	**ALL**: No DCI support for CScripts (NO FIX)
TT-16386	**JSL**: DCI gets wrong register values in Code window
TT-16183	**TGL-U**: When restore hardware breaks on reset is enabled, SourcePoint not able to stop the target
TT-16124	**ICX**: Power cycle support not functional

For SPR, note that the first reset of a Sapphire Rapids target after loading the SourcePoint project does not stop the target at the reset vector. To stop the target at the reset vector, power cycle it after loading the SP project. The Reset button should then work for the remainder of the debug session. Here are the steps:

1) Power on XDP3e
2) Power on Sapphire Rapids target
3) Start SP and load project
4) Turn off target
5) Turn on target
6) Click on the Reset button
7) Verify that the target halts at the reset vector

For ICX-D:
1. We have noted that, on some targets, it is necessary to increase the stability time after reset to successfully stop at the reset vector. In the Options menu, go to Emulator Configuration, select the Target Reset tab, and increase the “After target reset, emulator will wait….” from what may be the default of 100 milliseconds to 400 milliseconds.
2. With reset break set, the target does halt but with some slip, after issuing a reset from the target UEFI console (looks like a cold reset).
3. With init break or power cycle break set, the target resets but continues to boot (all the way to the UEFI console), after issuing a reset from the target UEFI console (looks again like a cold reset).
4. Setting power cycle break and power cycling the target locks up both SourcePoint and the target (i.e. no JTAG at all). The only way out of this is to quit the emulator, power

cycle the target, wait for it to begin booting and then bring back up the emulator again, at which point you can then turn the power cycle break off again.

A key erratum for JSL is the inability to halt the target at the Reset Vector via either a Power Breakpoint or a Reset Breakpoint.

Version 7.12 Build 33 – May, 2023

This build has the following major enhancements:

- Granite Rapids support – 1P and 2P
- Meteor Lake support. Tested on Meteor Lake-P. Power cycle and reset are not fully functional yet.
- Emerald Rapids support. Run contol is fully functional for EMR.
- Sapphire Rapids AET support. AET trace now supports dumping LBRs for individual event types.
- Sapphire Rapids support added for S3 stepping silicon.
- Alder Lake-N support added.
- New Project Wizard improvements. This has been streamlined and is easier to use.

Version 7.12 Build 22 – July, 2022

This build has the following major enhancements:

- UEFI macro enhancements for GCC compiler
- Sapphire Rapids-HBM support
- Sapphire Rapids R0, L0, L0 support
- VMExit and VMLaunch hypervisor breakpoint support
- Full Alder Lake support of all Core/Atom configurations, with Trace
- Enhancement to bitfield display for structures with union
- Rocket Lake DCI support
- Raptor Lake support
- Enhanced support for AET with LBR
- CScripts support for Python 3.6.x rather than Python 2.7.
- Peek Memory: allows the reading of 32 bits of data using a register as the memory address
- Find MSR feature: search the Register view for an MSR by number.

Version 7.12 Build 16 – September, 2021

7.12.16 has the following new features and fixes:

- Update to Visual Studio 2019 toolchain
- Python 3.x support for CScripts
- New Project Wizard with Target Identification
- Sapphire Rapids reset fix and support through E0 (PRQ) stepping
- Alder Lake big.little support
- ICX-D U0 support
- Software breakpoints for JSL and EHL fixed
- Multithread AP code execution segment register display fixed

Version 7.11

Build 113

ICX-D U0 Support - Run control support added for ICX-D U0.

JSL breakpoint issue - Software breakpoints are now functional on Jasper Lake.

EHL breakpoint issue - Software breakpoints are now functional on Elkhart Lake.

EHL register corruption issue - Certain general register values would get corrupted during PEI debug. This has been resolved.

Build 109

SPR B0 dual package issue - Fixed issue with CS and SS registers first thread in second package sometimes cleared after running to breakpoint.

Build 108

SPR B0 support - Run control support added for SPR B0 stepping

Build 107

ADL-S support - Run control support added for ADL-S. Only the Core cores are supported at this time. Atom cores are ignored.

Build 106

TGL R0 support - Run control support added for TGL R0 stepping

EHL RCX issue - Fixed issue with RCX sometimes cleared when running to hardware breakpoint

Build 103

ICX-D support - Run control support added for ICX-D Y0/U0 stepping

RKL Trace Hub support - Trace Hub support added for RKL

Eagle Stream CScripts support - Support added for Eagle Stream (SPR) CScripts

Build 102

TGL P0 support - Run control support added for TGL P0 stepping

Build 100

Rocket Lake (RKL-S) - Run control support added for RKL-S

SPR Trace support - LBR, BTS and Intel PT trace support added for SPR

Build 99

Elkhart Lake support (EHL) - Run control support added for EHL

ICX AET support - AET trace support added for Ice Lake Server

Build 97

Sapphire Rapids support (SPR) - Run control support added for SPR.

SKL-D support - Run control support added for SKL-D.

Build 96

Jasper Lake support (JSL) - Run control support added for JSL

Build 95

IceLake Server (ICX) C0 support - Run control support added for ICX C0 stepping.

NDA processor support - Intel processors still under NDA are now supported in the standard SourcePoint release. It's no longer required to visit the SourcePoint Community to download support files.

Build 91

Comet Lake (CML) P0 support - Run control support added for Comet Lake P0 stepping

Build 89

Comet Lake (CML) G0 support - Run control support added for Comet Lake G0 stepping

Comet Lake (CML) DbC support - Run control support (via DbC) added for Comet Lake

Tiger Lake (TGL) DbC support - Run control support (via DbC) added for Tiger Lake

DbC connection status utility - DbC connection utility now provided with SourcePoint release. This utility is useful for troubleshooting DbC connection issues. It indicates whether the host computer's DCI driver has a valid connection to the target.

IceLake server (ICX) trace support - LBR trace and Intel PT trace are now supported on ICX.

Build 80

Comet Lake (CML) support - Run control support added for Comet Lake

Tiger Lake (TGL) support - Run control support added for Tiger Lake

Build 79

IceLake Server (ICX) support - Run control support added for two-package ICX.

Build 76

Ice Lake Server (ICX) support - Run control support added for ICX. Single package only.

DCI support - Added support for DCI (DbC). Allows for debug through a USB connection (without a debug probe).

MCE Breakpoints - New MCE breakpoint type allows trigger on machine check exceptions

Version 7.10.4

5th Generation Intel® Xeon™ processor (codename Skylake) – SourcePoint now supports the new 5th Generation Intel® Xeon™ processor.

Windows 10 support

Gemini Lake Support – Added support for GLK processors

Coffee Lake Support – Added support for CFL processors (requires NDA)

Cannon Lake Support – Added support for CNL processors (requires NDA)

IceLake Support – Added support for ICL processors (requires NDA)

BSSB Trace – Added support for BSSB streaming trace (requires DCI connection)

CFL Trace – Added support for CFL trace (requires NDA). Includes Intel PT, Software trace through the Trace Hub, and AET trace through the Trace Hub.

CNL Trace – Added support for CNL trace (requires NDA). Includes Intel PT, Software trace through the Trace Hub, and AET trace through the Trace Hub.

VS 2015 Support - Added symbolic support for VS 2015 compiler.

Improved C-State Handling

ICL Trace - Added support for ICL trace (requires NDA). Includes Intel PT, Software trace through the Trace Hub, and AET trace through the Trace Hub.

LBR Trace Bug Fix – Fixed bug that resulted in incorrect LBR trace when going off of a breakpoint.

Version 7.10.3

Trace Hub Support - SourcePoint now supports software / firmware trace through the Intel Trace Hub to system memory.

Intel PT Timestamp - SourcePoint now supports TSC, MTC and TMA packets in Intel PT. This allows Intel PT from multiple cores to be time aligned.

Version 7.10.2

Intel Processor Trace Support – Added support for Intel Processor Trace (Intel PT). See the Trace view section for more information.

Trace Search View - The Trace Search view has been added to support Intel PT. This view supports high level views of the trace. The view can be opened from the Trace view context menu.

Trace Statistics View - The Trace Statistics view has been added to support Intel PT. This view supports function profiling of instruction trace data. The view can be opened from the Trace view context menu.

Version 7.10.1

IvyTown Support - Support added for IvyTown including ureg_raw command and Python-CLI device model.

Alternate Processor Numbering - SourcePoint now supports both the Arium and ITP processor numbering schemes. The ITP numbering scheme is selected by setting the ItpCompatible control variable true.

XDP-Pins - The LX-INT tab in the Emulator Configuration dialog has been reworked to support the new LX-INT rev E-1 adapter. The tab has been renamed "XDP-Pins"

GD Bit - SourcePoint now supports the GD bit in DR6 to break on target software modifying the DR registers.

Improved Program Load Verification - When verifying a program loaded symbols only, SourcePoint now allows individual sections to be excluded from the verify (e.g., the Init section in a Linux kernel load).

Version 7.10

Target Configuration – Target configuration is now handled by a series of new commands executed in the target configuration event macro. See the new Target Configuration Application Note for more information.

Python Support – SourcePoint now has limited support for the Python Command language.

1024 Processor Support – The number of processors (threads) supported has been increased from 64 to 1024.

Haswell Support – The Haswell processor is now supported including Haswell NI instructions.

Editing of Macro File Errors – The Macro error dialog now allows opening an editor to fix macro file errors, and then resumption of the macro.

SelectFile and SelectDirectory commands – These new commands open dialogs to allow a filename or directory path to be returned to an nstring variable.

Symbol Search Improvement – The Symbol Finder dialog (Edit | Find Symbol) now allows searching for a symbol across multiple programs.

Program Save Improvement – The Program Save dialog now allows for saving a region of memory as an axf file. The Save (Upload) command also supports this.

Viewpoint View Improvements – The Viewpoint window now allows sleeping processors to be automatically hidden from the display. It also allows for individual processors to be hidden.

The following target configuration commands have been added (see Target Configuration Application Note for more information)

- ***JtagTest***
- ***JtagScan***
- ***JtagConfigure***
- ***VerifyJtagConfiguration***
- ***UncoreScan***
- ***UncoreConfigure***
- ***DeviceScan***
- ***DeviceConfigure***
- ***VerifyDeviceConfiguration***
- ***Autoconfigure***
- ***Disconnect***
- ***Reconnect***

Emulator

The table below describes the behavior of the status LEDs on the front of the emulator.

STS	Lights briefly after emulator has performed boot-level hardware initialization and prior to loading flash image. Also, the upper and lower amber LEDs flash in an alternating pattern if the flash file fails to load.
RST	When lit, the target is in reset mode.
RUN	When lit, the target is running.
PWR	When lit, the emulator's power is on.

The table below describes the behavior of the network LEDs on the back of the emulator.

100BT	When lit, the emulator is communicating at 100Mb/s
LINK	When lit, indicates Ethernet is connected.
RECV	When lit, indicates Ethernet is receiving data.